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Thermal calibration procedure for internal infrared laser deflection apparatus

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A procedure to calibrate the temperature measurements in the transient regime of internal IR-laser deflection (IIR-LD) apparatus is presented. For this purpose, a thermal test chip (TTC), whose behavior is analytically well described by a simple model, is used. During the calibration process, the TTC is thermally excited during short heating times (up to 250 μs), estimating its internal temperature profile by IIR-LD measurements. Afterwards, experimental results and model predictions are compared. Good agreement between theory and experiment is found when a temperature rise ranging from 0 to 1.4 K is measured. The presented procedure can be also used to thermally calibrate optical probing apparatus for measuring the thermal behavior of power devices, as well as to determine thermal parameters of other materials, such as SiC and GaN. In particular, it should be very useful for the determination of the thermo-optical coefficient $(\partial n/\partial T)_C$ of such materials. In the present work, a value for $(\partial n/\partial T)_C$ of 2.0×10^{-4} K^{-1} is found in silicon, which agrees with literature reported values. The benefits of this method are its simplicity, accuracy, and low time consumption. © *2005 American Institute of Physics.* [DOI: 10.1063/1.2039687]

INTRODUCTION

In the past years, several techniques have been developed to measure the internal temperature of power devices, improving the spatial resolution achieved in the junction temperature measurement. One of them is the internal IR-laser deflection (IIR-LD) (Ref. 1). In this technique, an IR-laser probe beam goes through a biased device under test (DUT), striking on its lateral sides perpendicularly. From the measurement of the radiation absorption and beam deflection, it is possible to deduce a longitudinal averaged value for the temperature gradient and free-carrier concentration at a given depth.[2] The beam deflection is due to the refractive index gradient $\nabla_y n$ ("mirage" effect). The mirage effect is induced by the coupled contribution on $\nabla_y n$ of temperature and free-carrier concentration gradients $(\nabla_y T, \nabla_y C)$ inside the device, as described by

$$\nabla_y n = \left(\frac{\partial n}{\partial C}\right)_T \nabla_y C + \left(\frac{\partial n}{\partial T}\right)_C \nabla_y T, \tag{1}$$

where $(\partial n/\partial C)|_T$ and $(\partial n/\partial T)|_C$ denote the proportionality coefficients for free-carrier and temperature gradients, respectively. In the present work, only thermal effects will be considered $(\nabla_y C=0)$, as explained further. Taking into account that $\nabla_y n$ is proportional to the laser beam deflection signal $V_{\text{out},y}$ measured with a germanium four-quadrant photodetector, the $\nabla_y T$ at a given measurement depth can be written as[2]

$$\nabla_y T = \frac{\text{NA}}{\kappa' L\left(\frac{L}{2f_{L_2}n_0}+1\right)\left(\frac{\partial n}{\partial T}\right)_C} V_{\text{out},y}, \tag{2}$$

where NA is the laser beam numerical aperture, L is the device lateral dimension, κ' is a detection circuit constant, f_{L_2} is the focal length of a setup lens, and n_0 is the silicon refractive index at room temperature. Measuring $\nabla_y T$ at different depths, the internal temperature profile of the device can be evaluated integrating $\nabla_y T$ along the vertical direction. As can be observed from Eq. (2), several parameters are involved in the $\nabla_y T$ determination. Consequently, various error sources may appear in the proportionality factor determination, relating $V_{\text{out},y}$ with $\nabla_y T$. Therefore, a calibration procedure must be carried out.

In this work, a calibration procedure for the IIR-LD apparatus is presented. The method is based on a thermal test chip (TTC), whose behavior is well described by an analytical thermal model. Thus, from a direct comparison of the extracted temperature with the model prediction, the mentioned proportionality factor is determined.

THERMAL TEST CHIP

TTC structure description

As Fig. 1 shows, the TTC structure consists of a 525-μm silicon substrate (low doped) with polysilicon stripes distributed on its topside surface (6×6 mm^2), acting as a heating resistor. Two kinds of substrates have been used for the TTC manufacturing: N type (1×10^{14} cm^{-3}) and P

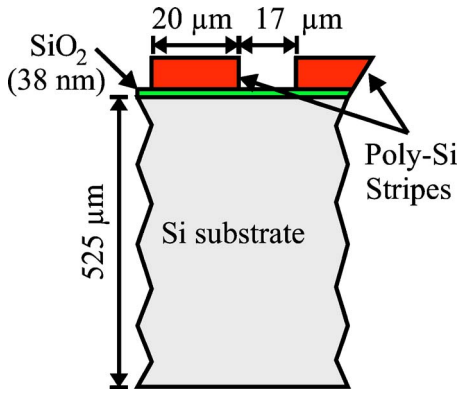

FIG. 1. Cross-sectional view of the TTC (not to scale).

type (1×10^{15} cm^{-3}). The stripes are interconnected in parallel obtaining a 60-Ω resistance value. Moreover, they are electrically isolated from the silicon substrate by a very thin SiO_2 layer (38 nm), practically not affecting the heat diffusion towards the silicon substrate. This stripe-shape topology of the heating resistor assures that the current density is uniformly distributed inside them, reaching a uniform heating of the substrate topside. The polysilicon stripes are 20 μm wide and 5.52 mm long, with a 17-μm separation between each stripe (see Fig. 1). These dimensions lead to achieve a perfect vertical heat flow from a given depth (30 μm, approximately), obtaining a one-dimensional (1D) temperature profile along the TTC depth, as shown further. The TTC preparation process starts by polishing its lateral sides, which interact with IR-radiation, enhancing its transmission. After that, the TTC is soldered on an insulator metal substrate (IMS) and the heating resistor contacts are established with aluminum wire bonds.

TTC simulated thermal behavior

In order to demonstrate that the stripe distribution of the heating resistor allows obtaining a 1D profile of temperature rise within the TTC, three-dimensional (3D) simulations using the FLOTHERM package[3] are performed. Figure 2 illustrates the used 3D structure for this purpose, corresponding to a part of the fabricated TTC. In this figure, it can be observed a substrate of 373×600 μm^2 lateral dimensions and 525 μm thickness, with ten polysilicon stripes (20 μm wide), on its topside, distanced 17 μm apart. The basic thermal behavior of the full size (6×6 mm^2) TTC can be understood with such a simplified structure, avoiding excessive simulation times. The thin SiO_2 layer, placed between the polysilicon and the silicon substrate, has not been taken into account in the performed simulations, since its transient thermal effects do not affect the heat-flow evolution at the time scale analyzed in the present work. Regarding the simulation conditions, a constant power has been dissipated for each stripe, deriving its value from the heat flux density dissipated on the full-sized TTC top (45 mW for each stripe corresponding to 60 W for the whole TTC). The initial temperature condition is room temperature (293 K), and the boundary conditions are adiabatic on the top surface of the simulated structure and isothermal surface on the bottom (293 K). The main simulation results are shown in Figs. 3 and 4.

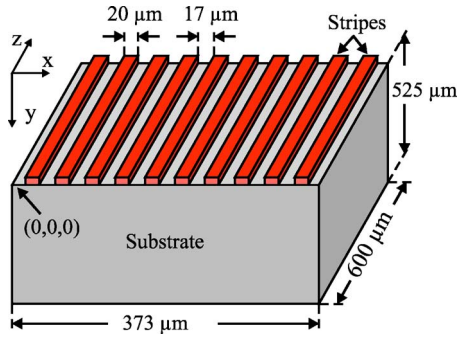

FIG. 2. Simulated 3D structure, part of the full size TTC, showing its dimensions (not to scale).

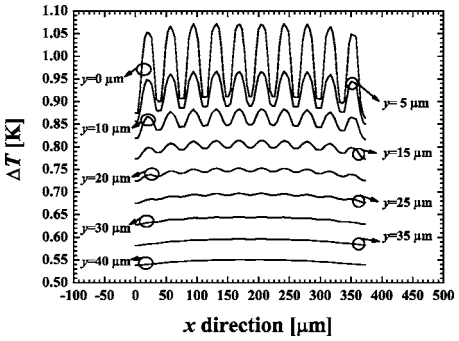

FIG. 3. Simulated temperature increase profile along the x direction for several depths at $t=50$ μs.

Figure 3 shows the temperature distribution along the x axis for several depths, ranging from $y=0$ to $y=40$ μm, at the time instant $t=50$ μs. As can be observed, the temperature distribution along x is almost constant from $y=30$ μm. Subsequently, a 1D temperature profile is approximately achieved from this depth inside the TTC. For this reason, all measurements will be performed from a 70 μm depth, assuring that a 1D profile of ΔT is well established.

In Fig. 4, the two-dimensional (2D) cross-sectional view of the temperature distribution corresponding to the x-y plane located at $z=300$ μm is shown at the time instant $t=250$ μs. As a main noticeable fact, the isothermal line cor-

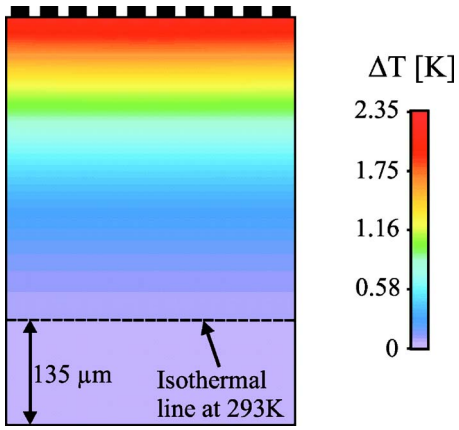

FIG. 4. 2D cross-sectional view of the simulated temperature distribution at $z=300$ μm and $t=250$ μs, showing that the isothermal line $T=293$ K is located 135 μm from the structure backside.

TABLE I. Reported values for $(\partial n/\partial T)_C$ used in this work.

$(\partial n/\partial T)_C$ (K^{-1})	Temperature conditions (K)	References
1.8×10^{-4}	288–308	Ref. 6
1.6×10^{-4}	Room temperature	Ref. 7
1.9×10^{-4}	Room temperature	Ref. 8
2.0×10^{-4}	Room temperature	Ref. 9

responding to $T=293$ K is 135 μm from the structure backside, indicating that the heat front has not reached it yet. Consequently, the TTC can be thermally considered as a semi-infinite medium. Moreover, a temperature rise below 2.5 K for $t=250$ μs is obtained for a 60 W equivalent power dissipated on the whole TTC top, also assuring that the involved thermal parameters, i.e., the thermal conductivity and diffusivity, remain constant.

TTC thermal modeling

According to simulation results from the previous section, the evolution of the temperature rise inside the TTC may be described using the solution of the 1D equation of heat conduction in a semi-infinite solid with a power source at $y=0$ dissipating a constant power P_0 in a given area A (Ref. 4):

$$\Delta T = -2\nabla_y T|_0 \left[\sqrt{\frac{\alpha t}{\pi}} \exp\left(\frac{-y^2}{4\alpha t}\right) - \frac{y}{2} \operatorname{erfc}\left(\frac{y}{\sqrt{4\alpha t}}\right) \right], \tag{3}$$

where $\nabla_y T|_0$ and α denote the steady-state temperature gradient and the thermal diffusivity of silicon, respectively. Moreover, $\nabla_y T|_0$ may be expressed as follows:

$$\nabla_y T|_0 = \frac{P_0}{Ak}, \tag{4}$$

where A and k correspond to the device active area (30 mm^2) and the thermal conductivity of silicon (0.148 W mm^{-1} K^{-1}) (Ref. 5), respectively. α may be derived from

$$\alpha = \frac{k}{\rho c}, \tag{5}$$

where ρ and c are the mass density of silicon (2.33×10^{-6} kg mm^{-3}) (Ref. 5) and the specific heat of silicon (713 J kg^{-1} K^{-1}) (Ref. 5), respectively.

THERMAL CALIBRATION

Procedure description

The calibration procedure will consist in estimating the temperature profile from a direct measurement, using Eq. (2), and comparing it with the model prediction of Eqs. (3)–(5). To evaluate Eq. (2), aside from directly involved apparatus parameters easily determined $(L,\kappa',n_0,NA,f_{L_2})$, the $(\partial n/\partial T)|_C$ value is also required. Subsequently, different values found in the literature,[6–9] summarized in Table I, are employed.

For the proposed calibration procedure, the selection of the model parameters k and α is critical. The selected values have been taken from the literature for the experimental conditions of this work. k shows the main contribution to the uncertainty of the model prediction, and a 10% variation of its value is found depending on the different references. Nevertheless, Eq. (3) is very robust under the variation of this parameter. Namely, when k experiences a 10% variation, the temperature prediction shows a variation below 2% for all observed depths (from $y=70$ μm to $y=495$ μm). This fact is a direct consequence of the decreasing exponentials that nullifies the effect of k^{-1} dependence of Eq. (3).

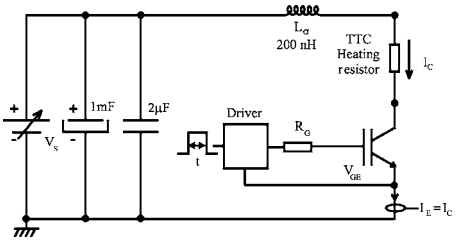

FIG. 5. Schematic of the TTC connection to the excitation circuit.

The heating process parameters, i.e., dissipated power and heating time (t), are controlled by the excitation circuit presented in Fig. 5 (Ref. 10). As shown in the figure, this circuit is formed by an insultated gate bipolar transistor (IGBT), its gate driver, gate resistors (R_G), the TTC, and two decoupling capacitors to assure pulsed current levels up to 25 A for a voltage source (V_S) up to 300 V. Furthermore, the conduction time can be controlled between 10 and 500 μs by means of a 33120A Hewlett Packard function wave-form generator. The dissipated power is established by the level of the current pulse I_C conducted in the polysilicon stripes (Joule effect), which is adjusted through the V_S voltage. As experimental conditions, a maximum heating time of 250 μs has been chosen to be in the validity conditions of Eq. (2), as previously mentioned. Regarding the dissipated power on the TTC top, a maximum value of 60 W is selected. In such conditions, the thermal conductivity and diffusivity remain constant because of the low values of temperature increase reached inside the TTC.

Measured signals and $(\partial n/\partial T)_C$ selection

In the same experimental conditions, the obtained results for N- and P-type TTC substrates do not diverge excessively between them. For this reason, only some results corresponding to the measured $V_{\text{out},y}$, as well as the influence of the

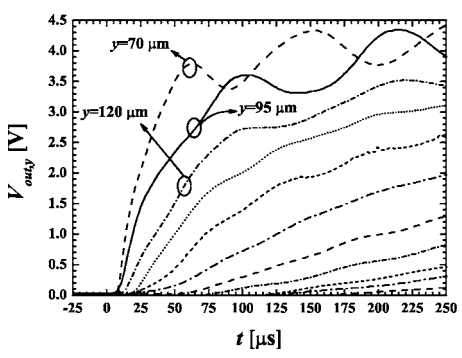

FIG. 6. Heating time dependence of the measured $V_{\text{out},y}$ wave forms at different measurement depths inside the N-type TTC.

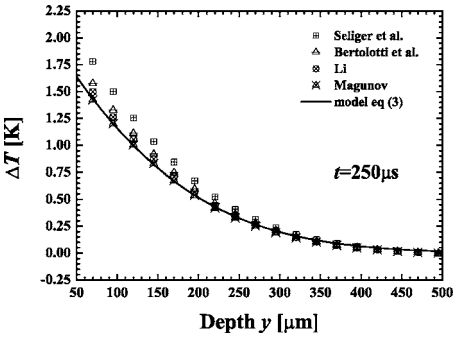

FIG. 7. Extracted temperature profile evaluated for $(\partial n/\partial T)_C$ reported values and its comparison with the prediction of Eq. (3) for $t=250$ μs.

thermo-optical coefficient values to ΔT estimation, are shown for the *P*-type TTC. Figure 6 shows the time evolution of $V_{\text{out},y}$ at the various depths considered in this work during a heating time of 250 μs for $P_0=60$ W. As inferred from Eq. (2), note that $\nabla_y T$ follows the same behavior as $V_{\text{out},y}$. For measuring depths close to the chip top (70, 95, and 120 μm), $V_{\text{out},y}$ presents oscillations. They are due to interference phenomena on the detector surface, as a result of the superposition of the probe beam (main ray) with its multiple reflections into the TTC lateral sides.[11] Its origin is a consequence of the refractive index increase with temperature, which changes the optical path between all the interacting rays (Fabry-Perot interference). This effect is more important closer to the heat source, since the temperature increase is higher.

Figure 7 depicts the vertical temperature profile for $t=250$ μs evaluated using different $(\partial n/\partial T)_C$ coefficient values from the literature. In this case, all the values of Table I

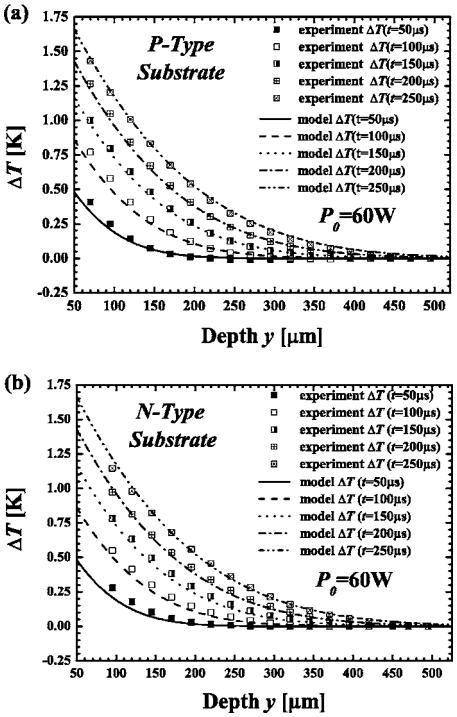

FIG. 8. Extracted temperature profile compared with the prediction of Eq. (3) for several heating times, using $(\partial n/\partial T)_C$ Magunov's value, for (a) *P*-type substrate and (b) *N*-type substrate.

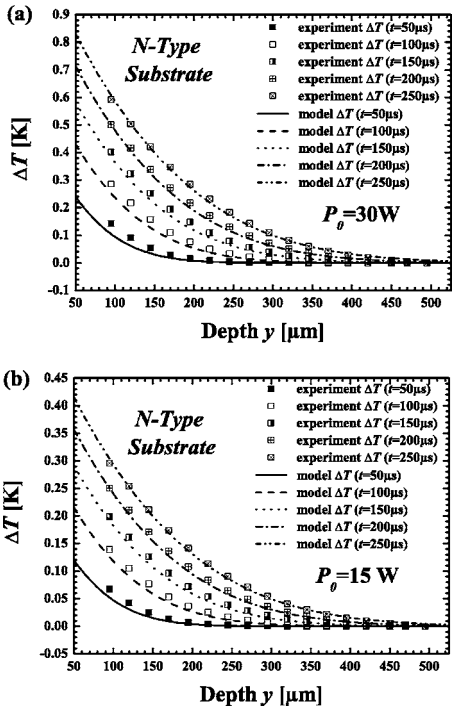

FIG. 9. Comparison between the model results and the extracted temperature profile from the *N*-type TTC for (a) $P_0=30$ W and (b) $P_0=15$ W for several heating times, using $(\partial n/\partial T)_C$ Magunov's value.

are used to evaluate Eq. (2). The best agreement with the theoretical model is achieved considering Magunov's coefficient value[9] being the most suitable thermo-optical coefficient in the present case. It can be observed that the estimated ΔT using Magunov's, Bertolotti's, and Li's reported values is agreed among them and diverge from the estimation corresponding to Seliger's coefficient when their experimental error is considered. This difference might arise from the experimental method followed by Seliger *et al.* While the former measured both the refractive index and the temperature variation for $(\partial n/\partial T)_C$ determination, Seliger *et al.* obtained this value comparing Fabry-Perot interference measurements with a simulated temperature profile.[12]

Temperature rise measurements

Once the suitable thermo-optical coefficient is found, ΔT can be measured in both kinds of TTC substrates. Thus, aside from direct comparison between the 1D model and measurements, the obtained results may be verified. This is possible since $(\partial n/\partial T)_C$ does not depend on doping level,[9,13] and, subsequently, the thermal proportionality factor is not affected. Figure 8 presents the model prediction on ΔT and the experimental results using the Magunov's coefficient for different heating times. These results are contrasted for each TTC type, presenting the *P*-type case in Fig. 8(a) and the *N*-type in Fig. 8(b). As can be observed, a very good agreement between theory and experiment is obtained.

For further verification, ΔT inside the *N*-type TTC is also measured for two different P_0 values and compared with the model prediction, as shown in Fig. 9. Concretely, Figs. 9(a) and 9(b) depict ΔT comparison for $P_0=30$ and 15 W, respectively, ranging the heating time from 50 to 250 μs.

From these results, it can be observed that the measured ΔT in both cases are scaled by a factor of 2, which corresponds to the ratio between dissipated powers. This fact agrees with theory as it can be inferred from Eq. (3), where, at a given time, the ΔT value only depends on the dissipated power. In both cases, the difference between measurements and model prediction is 17% for $t=50$ μs, but, from $t=150$ μs, it is drastically reduced below 5%. This higher difference for short heating times ($t=50$ μs and $t=100$ μs) can be associated with experimental limitations. However, the accuracy of this technique allows, inside a 6×6 mm^2 chip, ΔT measurements as low as 100 mK with a discrepancy from the model prediction of 17 mK.

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